AMENDMENTS TO THE CLAIMS

Please cancel claims 21 and 35 without prejudice.
The following listing of claims replaces all previous versions of the claims.

1. (Currently Amended) An apparatus comprising:

a memory element in a processor to supply a configured clock rate setting for use by a peripheral set;

an input element in the processor to receive a feedback clock rate setting from the peripheral set, said feedback clock rate setting being bundled with a plurality of power-on-configuration (POC) signals received in response to a reset of the processor; and

a comparison unit in the processor to compare the configured clock rate setting and the feedback clock rate setting to detect over-clocking of the processor.

2. (Original) The apparatus of claim 1 wherein the memory element comprises at least one fuse, said at least one fuse being one-time configurable with the configured clock rate setting.

3. (Original) The apparatus of claim 1 wherein the input element comprises at least one digital register, said at least one digital register being dynamically re-written for each reset of the processor.

4. (Original) The apparatus of claim 1 further comprising:

a control unit in the processor to place the processor in a detected state if the comparison unit detects over-clocking.

5. (Original) The apparatus of claim 4 further comprising:

a second memory element in the processor to store a detection enable setting, said control unit to place the processor in the detected state if both the over-clocking is detected and the detection enable setting is enabled.

6. (Original) The apparatus of claim 5 wherein the second memory element comprises a fuse, said fuse being one-time configurable with the detection enable setting.

7. (Original) The apparatus of claim 4 wherein the detected state comprises one of a low frequency mode and a shut down mode.

8. (Original) The apparatus of claim 4 wherein the control unit is further to output an over-clocked detection signal from the processor if the comparison unit detects over-clocking.

9. (Original) The apparatus of claim 1 further comprising:

an output port on the processor for the configured clock rate setting; and

a tri-state unit in the processor, coupled between the memory element and the output port, said tri-state unit to place the output port in a tri-state subsequent to a reset of the processor.

10. (Original) The apparatus of claim 9 further comprising:

a second memory element to store a tri-state enable setting; and

an enable unit to enable the tri-state unit based on the tri-state enable setting and a second signal asserted a particular time subsequent to the reset of the processor.

11. (Original) The apparatus of claim 10 wherein the enable unit comprises a logical AND of the tri-state enable setting and the second signal.

12. (Original) The apparatus of claim 1 wherein the configured clock rate setting and the feedback clock rate setting each comprise digital codes of at least one bit each, and wherein the comparison unit comprises a digital comparator.

13. (Original) The apparatus of claim 1 further comprising:

the peripheral set.

14. (Original) The apparatus of claim 13 wherein the peripheral set comprises at least one of a clock generator, a memory, an input/output interface, a memory controller hub, and an input/output controller hub.

15. (Currently Amended) An apparatus comprising:

a clock generator to generate a clock signal based on a clock rate setting, and said clock rate generator to provide the clock signal for use by a processor, said processor ~~having~~ to provide a configured clock rate setting for use by the clock generator; and

a clock rate feedback unit to generate a feedback clock rate setting based on a clock rate of the clock signal, and said clock rate feedback unit to ~~provide the feedback clock rate back for use by~~ bundle the feedback clock rate setting with a plurality of power-on-configuration (POC) signals provided to the processor in response to a reset of the processor, said feedback clock rate setting for comparison to the configured clock rate setting to detect over-clocking.

16. (Currently Amended) The apparatus of claim 15 wherein the clock rate feedback unit comprises one of:

a circuit within the clock generator;

~~a circuit within the processor;~~ and

a circuit within a memory controller hub, said memory controller hub to couple with both the clock generator and the processor.

17. (Original) The apparatus of claim 15 wherein the clock rate feedback unit comprises one of:

a frequency measurement circuit to measure a frequency of the clock signal; and

a register to store a code indicating a current clock rate setting of the clock generator.

18. (Original) The apparatus of claim 15 wherein the clock generator and the clock rate feedback unit comprise a peripheral set to couple with the processor.

19. (Original) The apparatus of claim 15 further comprising:

a memory element to store the clock rate setting during each reset of the processor.

20. (Original) The apparatus of claim 15 further comprising:

a memory controller hub comprising at least one of the clock generator and the clock rate feedback unit; and

a front side bus to couple the memory controller hub with the processor.

21. (Cancelled)

22. (Currently Amended) A system comprising:

a processor;

a clock generator to generate a clock signal for the processor based on a clock rate setting; and

a memory controller hub to supply a feedback clock rate setting based on a clock rate of the clock signal, said feedback clock rate setting being bundled with a plurality of power-on-configuration (POC) signals generated in response to a reset of the processor;

said processor comprising

a memory element to provide a configured clock rate setting for use by the clock generator,

an input element to receive the feedback clock rate setting from the memory controller hub, and

a comparison unit to compare the configured clock rate setting and the feedback clock rate setting to detect over-clocking of the processor.

23. (Original) The system of claim 22 wherein the processor further comprises:

a control unit to place the processor in a detected state if the comparison unit detects over-clocking.

24. (Original) The system of claim 23 wherein the detected state comprises one of a low frequency mode and a shut down mode.

25. (Currently Amended) A method comprising:

providing a configured clock rate setting from a processor for use by a peripheral set;

receiving a feedback clock rate setting at the processor from the peripheral set, said feedback clock rate setting being bundled with a plurality of power-on-configuration (POC) signals generated in response to a reset of the processor; and

comparing the configured clock rate setting and the feedback clock rate setting to detect over-clocking of the processor.

26. (Original) The method of claim 25 wherein comparing comprises:

determining if the feedback clock rate setting is higher than the configured clock rate setting.

27. (Original) The method of claim 25 further comprising:

configuring a memory element in the processor with the configured clock rate setting prior to providing the configured clock rate setting.

28. (Original) The method of claim 27 wherein configuring the memory element comprises:

blowing at least one fuse.

29. (Original) The method of claim 25 wherein receiving the feedback clock rate setting comprises:

storing the feedback clock rate setting to a memory element in the processor for each reset of the processor.

30. (Original) The method of claim 25 further comprising:

placing the processor in a detected state if over-clocking is detected.

31. (Original) The method of claim 30 wherein placing the processor in the detected state comprises:

asserting an enforce signal if over-clocking detection is enabled;

asserting a detection signal if over-clocking is detected; and

initiating the detected state if both the enforce signal and the detection signal are asserted.

32. (Original) The method of claim 30 wherein the detected state comprises one of a low frequency mode and a shut down mode.

33. (Original) The method of claim 30 wherein placing the processor in the detected state comprises:

outputting an over-clocked detection signal from the processor.

34. (Original) The method of claim 25 wherein providing a configured clock rate setting comprises outputting a configured setting signal from the processor, the method further comprising:

tri-stating the configured setting signal at a particular time subsequent to the reset of the processor.

35. (Cancelled)

36. (Currently Amended) A method comprising:

generating a clock signal at a peripheral set based on a clock rate setting;

providing the clock signal from the peripheral set for use by a processor, said processor ~~having~~ to provide a configured clock rate setting for generating the clock signal; ~~and~~

generating a feedback clock rate setting based on a clock rate of the clock signal for use by the processor for comparison to the configured clock rate setting to detect over-clocking;

bundling the feedback clock rate setting with a plurality of power-on-configuration (POC) signals generated in response to a reset of the processor; and

providing the POC signals to the processor following the reset.

37. (Original) The method of claim 36 wherein generating the feedback clock rate setting comprises one of:

measuring a frequency of the clock signal; and

reading a register storing a code indicating a current clock rate setting of the clock signal.

38. (Original) The method of claim 36 further comprising:

storing the clock rate setting during each reset of the processor.

39. (Currently Amended) A machine readable medium having stored thereon machine executable instructions, the execution of which to implement a method comprising:

providing a configured clock rate setting from a processor for use by a peripheral set;

receiving a feedback clock rate setting at the processor from the peripheral set, said feedback clock rate setting being bundled with a plurality of power-on-configuration (POC) signals generated in response to a reset of the processor; and

comparing the configured clock rate setting and the feedback clock rate setting to detect over-clocking of the processor.

40. (Original) The machine readable medium of claim 39 wherein the method further comprises:

placing the processor in a detected state if over-clocking is detected.

41. (Currently Amended) The machine readable medium of claim 39 wherein the method further comprises:

generating a clock signal at the peripheral set based on a clock rate setting;

providing the clock signal from the peripheral set for use by the processor; ~~and~~

generating the feedback clock rate setting based on a clock rate of the clock signal;

bundling the feedback clock rate setting with the POC signals; and

providing the POC signals to the processor following the reset.